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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/351,544	07/12/99	CARNS	T ZILG.204US0

EXAMINER	
ART UNIT	PAPER NUMBER
2815	

028345
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MM91/0326

DATE MAILED: 03/26/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/351,544	Applicant(s) CARNS ET AL.	
	Examiner Paul E Brock II	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 – 3, 8 – 12 and 13 – 25, have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

2. The indicated allowability of claims 4 – 7 and 26 – 30 are withdrawn in view of the newly discovered reference(s) to Watanabe (USPAT 6200846-B1), Havemann and Filipial et al. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claim 13 rejected under 35 U.S.C. 102(a) as being anticipated by Watanabe (USPAT 6200846-B1).

In regard to claim 13, Watanabe discloses a method of forming a capacitor in an integrated circuit with a bottom electrode layer (6) over a semiconductor body (2), forming a dielectric layer (7) over a portion of the bottom electrode, and a top electrode layer (8) over a portion of the dielectric layer as shown in figure 1a. A portion of the top electrode layer is removed to expose a portion of the dielectric layer (7), and an insulating layer (10) is formed over at least a portion of the top electrode (8a), and the exposed portion of the dielectric layer (7) as shown in figures 1b and 3a. Figures 1c and 3b further disclose removing a portion of the

insulating layer and a portion of the dielectric layer, thereby exposing at least a portion of the lower electrode layer and forming side wall spacers (10a), wherein the side wall spacers are formed on the side walls of the top electrode (8a) and of the inter-electrode region of the dielectric (7a).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (USPAT 6200846-B1) in view of Nishihori et al.

Watanabe discloses a method for forming a capacitor in an integrated circuit in figures 5a – 6b.

Watanabe discloses in figure 5a forming a bottom electrode layer (103) on a semiconductor body (100). The bottom electrode layer is also a conductive layer. Watanabe discloses in figure 5a forming a dielectric layer (104) over at least a portion of the bottom electrode layer. Watanabe discloses in figure 5a forming a top electrode layer (105) over at least a portion of the dielectric layer. Watanabe discloses in figure 5b removing a portion of the top electrode layer to expose a portion of the dielectric layer. Watanabe discloses in figure 5c subsequently forming a conformal insulating layer (106) over at least a portion of the exposed portion of the dielectric layer and at least a part of the top electrode layer proximate to the exposed dielectric layer. Watanabe discloses in figure 6b subsequently etching the bottom electrode layer. Watanabe does not disclose removing a portion of the exposed portion of the

dielectric layer before depositing a conformal insulating layer. Nishihori et al. teaches in figure 12a and 12b removing at least a portion of an exposed portion of a dielectric layer (44) to expose a portion of a lower electrode after removing a portion of a top electrode layer (45). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the method of subsequently removing at least a portion of an exposed portion of a dielectric layer of Nishihori et al. in the method of Watanabe in order to form an upper electrode and a dielectric layer of a capacitor with the same mask pattern as is well known in the art. It is thus apparent in the method of Watanabe and Nishihori et al. that forming the conformal insulating layer of over the structure that is resulted after the upper electrode and dielectric layers are defined would include subsequently forming a conformal insulating layer over at least a portion of the exposed portion of the bottom electrode layer proximate to the exposed dielectric layer, the exposed dielectric layer and at least part of the top electrode layer proximate to the exposed dielectric layer. It is also apparent that the above described steps would have formed a capacitor structure with a top electrode over a poriton of the conductive layer and a dielectric layer between the top electrode and the conductive layer, and a conformal insulating layer has been formed over the capacitor structure and at least a portion of the conductive layer proximate to capacitor structure. It is inherent that the conformal insulating structure has a thickness in the range from 20Å to 70Å.

7. Claims 2 – 4, 7 – 10, 12, 32, 33, 35 – 37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Nishihori et al. as applied to claims 1 and 31 above, and further in view of Filipiak et al.

With regard to claims 2, 32 and 33, Watanabe, in the Prior art embodiment used for claim 1, and Nishihori et al. do not disclose forming an antireflective layer over at least a portion of the resultant structure before etching the bottom electrode layer. Watanabe does disclose in figures 3c and 3d forming an anti-reflective layer (20) over at least a portion of a resulting structure prior to etching a bottom electrode (6a). It would have been obvious to one of ordinary skill in the art at the time of the present invention to form the antireflective layer of Watanabe over at least a portion of a resulting structure subsequent to forming the conformal insulating layer of Watanabe, in the Prior art embodiment used for claim 1, and Nishihori et al. in order to form resist patterns with good reproductivity as stated by Watanabe in column 7, lines 2 – 4. Watanabe and Nishihori et al. do not disclose the use of a conductive antireflective layer. Filipiak et al. does disclose the use of a conductive antireflective layer of TiN in column 1, lines 18 – 20. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the titanium nitride, conductive antireflective film of Filipiak et al. in the process of Watanabe and Nishihori et al. in order to reduce the likelihood of printing problems as stated by Filipiak et al. in column 1, lines 16 – 18.

With regard to claims 3, 8, 9, Watanabe, Nishihori et al. and Filipiak can be applied in the same manner as one would use to combine these references as if claims 1 and 2 were combined.

With regard to claim 4, Watanabe, Nishihori et al. and Filipiak can be applied in the same manner as one would use to combine these references as if claims 1 and 2 were combined, and it is inherent that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å.

With regard to claims 36 and 37, Watanabe, Nishihori et al. and Filipiak can be applied in the same manner as one would use to combine these references as if claims 31 - 33 were

combined, where it is inherent that a pattern mask is formed over the structure after forming the antireflective layer, the conductive layer is etched using the patterned mask, and it is inherent that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å.

With regard to claim 7, Watanabe discloses in column 1, line 42 that the conformal insulating layer is formed by deposition.

With regard to claim 10, Watanabe, Nishihori et al. and Filipiak do not disclose a method for depositing the anti-reflective layer as applied to claims 1-3 above. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a plasma enhanced chemical vapor deposition anti-reflective layer in order to deposit the anti-reflective layer.

With regard to claims 12, 35 and 39, Watanabe discloses in figures 5a – 6b that the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

8. Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Nishihori et al. and Filipiak et al.

Watanabe discloses in figure 3a forming a conductive layer (6) on a semiconductor body. Watanabe discloses in figure 3c forming an anti-reflective layer (20) over at least a portion of the conductive layer. Watanabe discloses in figure 3c forming a patterned mask (21a – 21c) over the antireflective layer, wherein the photolithographic process is optimized for forming the gates (6b and 6c). Watanabe discloses in figure 3d forming one or more capacitor structures, each comprising a top electrode (8a) over a portion of the conductive layer (6a) and a dielectric layer (7a) between the top electrode and the conductive layer. Watanabe does not disclose in figures

3a – 3d forming a conformal insulating layer over the capacitor structure before forming the antireflective layer. Watanabe does disclose in figures 5a – 5c forming a conformal insulating layer (106) over a capacitor structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the conformal insulating layers of Watanabe from figures 5a – 5c in the process of Watanabe in figures 3a – 3c in order to protect the surface of the underlying capacitor structure. It would thus be apparent that the antireflective layer would be formed on top of the conformal insulating layer and the conformal insulating layer would be over the capacitor structures and at least a portion of the conductive layer proximate to capacitor structures, wherein the capacitor formation process is performed prior to forming the antireflective layer, whereby the antireflective layer is additionally formed over the capacitor structures, and whereby the conformal insulating layer is formed such that the provided process flow is unaltered. Watanabe discloses in figure 3d etching the conductive layer according to the process flow, whereby the lower electrodes of the capacitor structures and the gates are formed. It is inherent that the conformal insulating layer has a thickness in the range from 20Å to 70Å.

9. Claims 5, 6, 34 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe, Nishihori et al. and Filipiak as applied to claims 4 and 33 above, and further in view of Havemann.

With regard to claim 5, 34 and 38, Watanabe, Nishihori et al. and Filipiak do not disclose that the conformal insulating layer is an oxide layer formed in a thermal process. Havemann teaches in column 5, lines 16 – 18 a thermal oxide layer deposited as a conformal insulating layer. It would have been obvious to one of ordinary skill in the art at the time of the present

invention to use the conformal insulating layer of thermal oxide of Havemann in the process of Watanabe, Nishihori et al. and Filipiak in order to provide minimal protection for the substrate as stated by Havemann in column 5, lines 18 – 21.

With regard to claim 6, it is inherent that the thermal process used to form the thermal oxide layer of Havemann is a rapid thermal oxidation performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe, Nishihori et al. and Filipiak as applied to claims 3 and 10 above, and further in view of Randazzo.

Watanabe, Nishihori et al. and Filipiak do not disclose the use of the plasma enhanced chemical vapor deposition anti-reflective layer having a thickness in the range from 300 to 400 angstroms. Randazzo teaches in column 4, lines 45-47 an anti-reflective layer having a thickness in the range of 300 to 400 angstroms. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use plasma enhanced chemical vapor deposition of Randazzo for depositing the anti-reflective layer of Watanabe, Nishihori et al. and Filipiak in order to have the thickness of the conductor in a desirable range.

11. Claims 14 – 21, 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (USPAT 6200846-B1) as applied to claim 13 above, and further in view of Filipiak et al.

In regard to claims 14, 15, and 21, an anti-reflective layer (20) is formed over at least a portion of the resultant structure after removing a portion of the insulating layer and a portion of the dielectric layer as illustrated in figure 3c of Watanabe. Watanabe does not disclose that the antireflective layer is a non-insulating layer. Filipiak et al. does disclose the use of a non-insulating antireflective layer of TiN in column 1, lines 18 – 20. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the titanium nitride, conductive antireflective film of Filipiak et al. in the process of Watanabe in order to reduce the likelihood of printing problems as stated by Filipiak et al. in column 1, lines 16 – 18. It is inherent that an anti reflective layer is also an antireflective coating.

In regard to claims 16 – 18, it is inherent to believe that the insulating layer (7) of Watanabe can be formed by deposition or by being grown. It is inherent that an anneal is performed after an insulating layer is formed by deposition.

With regard to claim 19, Watanabe discloses the use of an oxide layer with a thickness of 2500 angstroms as the insulating layer in column 8, lines 42-45. Watanabe and Filipiak et al. do not teach an oxide layer of thickness 500-2000 angstroms. With regard to claim 19, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the 2500 angstrom thick oxide layer of Watanabe to achieve the claimed thickness of 2000 angstroms since such changes in dimensions need no undue experimentation.

With regard to claim 20, the spacer width is determined by the thickness of the oxide layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to have a side wall spacer thickness in the range of 500 to 2000 angstroms which is equal to the thickness of the oxide layer of claim 19 above.

With regard to claim 23, Watanabe and Filipiak et al. do not disclose a method for depositing the anti-reflective layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a plasma enhanced chemical vapor deposition anti-reflective layer in order to deposit the anti-reflective layer.

With regard to claim 25, Watanabe discloses the bottom electrode layer additionally being used to form the gate of one or more transistors on the integrated circuit in figures 3c and 3d.

12. Claims 26 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Filipiak et al.

With regard to claims 26 – 30, Watanabe discloses in figure 5a forming a bottom electrode layer (103) on a semiconductor body (100). Watanabe discloses in figure 5a forming a dielectric layer (104) over at least a portion of the bottom electrode layer. Watanabe discloses in figure 5a forming a top electrode layer (105) over at least a portion of the dielectric layer. Watanabe discloses in figure 5c forming a nitride layer (106) over at least a portion of the top electrode and the exposed portion of the dielectric layer. Watanabe discloses in figure 5b removing a portion of the top electrode layer to expose a portion of the dielectric layer. Watanabe discloses in figure 6b subsequently removing a portion of the exposed portion of the dielectric layer and a portion of the bottom electrode layer, thereby exposing at least a portion of the semiconductor body and forming one or more capacitors. Watanabe does not disclose that the nitride layer is an anti-reflective layer. Filipiak et al. discloses an antireflective layer of titanium nitride instead of a nitride layer in column 1, lines 18 – 20. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the titanium nitride

antireflective film of Filipiak et al. in the process of Watanabe in order to reduce the likelihood of printing problems as stated by Filipiak et al. in column 1, lines 16 – 18. It is inherent that an anti reflective layer is also an antireflective coating. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a plasma enhanced chemical vapor deposition anti-reflective layer in order to deposit the anti-reflective layer. Watanabe discloses the bottom electrode layer additionally being used to form the gate of one or more transistors on the integrated circuit in figures 6a and 6c.

13. Claims 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (USPAT 6200846-B1) and Filipiak et al. as applied to claims 13-15 and 23 above, and further in view of Randazzo.

In regard to claims 22 and 24, Watanabe and Filipiak et al. do not disclose the thickness of the antireflective layer or the use of titanium nitride as an anti-reflective layer. Randazzo teaches the use of an anti-reflective layer of titanium nitride with a thickness in the range of 300-400 angstroms (column 4, lines 45-47). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the 300-400 angstrom thick, titanium nitride, anti-reflective layer of Randazzo as the anti-reflective layer of Watanabe and Filipiak et al. in order to form a barrier layer between the top electrode and a metal contact.

14. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Filipiak et al. as applied to claims 40 and 41 above, and further in view of Havemann.

Watanabe and Filipiak do not disclose that the conformal insulating layer is an oxide layer formed in a thermal process. Havemann teaches in column 5, lines 16 – 18 a thermal oxide

layer deposited as a conformal insulating layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the conformal insulating layer of thermal oxide of Havemann in the process of Watanabe and Filipiak et al. in order to provide minimal protection for the substrate as stated by Havemann in column 5, lines 18 – 21.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
March 21, 2001

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